High-Speed QPSK Modulator and Demodulator with Subharmonic Pumping

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Abstract—**High-speed modulators and demodulators which operate at gigabit transmission rates are essential components in many high-capacity communication links. We describe a subharmonically pumped QPSK modulator and demodulator using pairs of beam-leaded Schottky diodes and appropriate high-pass and low-pass filters on dielectric substrates. A modulator and a demodulator were operated in cascade at a carrier frequency of 13 GHz with a common pump at 6.5 GHz. This circuit showed clean eye diagrams of the recovered data trains up to 1.5 Gbit/s with corresponding error rates of less than 10^{-11}. The circuits can be readily scaled to higher frequencies with a proportional increase of the information rate.**

I. Introduction

A NEW TYPE of high-speed QPSK modulator/demodulator has been devised and constructed for use in digital communication links operating at gigabit per second transmission rates. Inherent in the modulator is the multiplexing of two baseband data streams each having bit rates up to half the maximum information rate. The basic modulator circuit can also demodulate and demultiplex the QPSK signal into the component bit streams entering the modulator. The microwave circuitry is broad-band, and the frequency range of operation is determined primarily by the local oscillator circuit which operates at one half of the carrier frequency. The basic circuit, with the exception of the nonlinear semiconductor elements, can be scaled dimensionally to other frequency ranges. Scaling to higher frequencies increases the maximum information rate proportionately.

Modulators which operate at high data rates and frequencies have been reviewed in detail by Cuccia and Mathews [1]. These circuits employ well-known digital modulation schemes treated by Sinnema [2], Greenstein and Fitzgerald [3], and Leuenberger [4], [5]. The major difficulty in building QPSK modulators which operate at gigabit per second rates is the design and construction of the filters and components which add the bit streams and local oscillator frequency at the input, and transmit and add the up-converted signals at the output. We show that these functions can be readily achieved with microstrip and finline components on a single substrate. A unique feature of this modulator design is the use of a subharmonic local oscillator frequency. This relaxes the requirements on the filters and makes higher frequency modulator circuits more practical. We also demonstrate that the bit error rates of the new modulator circuit are less than 10^{-11}, which makes it suitable for use in digital communication links.

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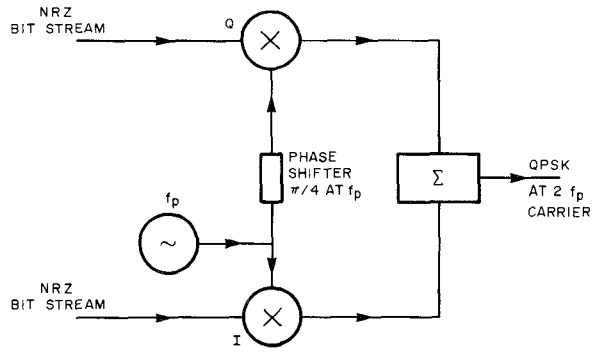

Fig. 1. Schematic view of QPSK modulator showing two rails with incoming NRZ bit streams, subharmonic local oscillator f_p, up-converting mixer circuits, and summing network at the output.

A prototype modulator–demodulator pair has been constructed for a carrier frequency of 13 GHz with a maximum design information rate of 2 Gbit/s. The performance of each unit has been evaluated and adjusted to give satisfactory performance with a single tuning element in the local oscillator circuits. Bit error rates were measured for transmission of pseudorandom data streams through the modulator-demodulator pair.

II. Theory of Operation

A simplified schematic of the modulator is shown in Fig. 1. Two bit streams enter the modulator in the in-phase (I) and quadrature (Q) ports. Each of these baseband signals has two states with the same amplitudes but with different polarities. The mixing elements have antisymmetrical nonlinear characteristics which are realized by pairs of paralleled, opposed Schottky diodes. If parasitic elements are neglected, the current–voltage characteristic for two identical ideal Schottky diodes connected in antiparallel may

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be represented by

$$i = i_0 \sinh(kv) \tag{1}$$

where i_0 and k are constants depending upon the diode construction.

The applied voltage to each mixing element is

$$v = v_p \cos(\omega_p t - m\pi/4) + v_b \tag{2}$$

where v_p and ω_p are the local oscillator amplitude and angular frequency, $m = 0$ for the in-phase mixer and $m = 1$ for the quadrature mixer, and v_b is the amplitude of the baseband input signals coded in non-return-to-zero (NRZ) format. A substitution of (2) into (1) leads to the desired output frequency components centered about the second harmonic of the local oscillator frequency. After some mathematical manipulation these components are

$$\left.\begin{matrix} i_I \\ i_Q \end{matrix}\right\} = 2i_0 \sinh(\pm kv_b) I_2(kv_p) \left\{\begin{matrix} \cos(2\omega_p t) \\ \cos(2\omega_p t - \pi/2). \end{matrix}\right. \tag{3}$$

In these expressions $I_2(kv_p)$ is a modified Bessel function of the first kind [6]. Both mixers have two states which are 180° apart in phase, corresponding to each of the two signs. Summing the currents from the two mixers gives four quadrature components of equal amplitude.

$$\left.\begin{matrix} i_1 \\ i_2 \\ i_3 \\ i_4 \end{matrix}\right\} = 2(2)^{1/2} i_0 \sinh(kv_b) I_2(kv_p) \left\{\begin{matrix} \cos(2\omega_p t - \pi/4) \\ \cos(2\omega_p t - 3\pi/4) \\ \cos(2\omega_p t - 5\pi/4) \\ \cos(2\omega_p t - 7\pi/4). \end{matrix}\right. \tag{4}$$

Equations (3) and (4) are obvious oversimplifications of a physically realizable circuit, but they indicate the origins of the quadrature components. Since each of the four components is the vector sum of two signals, each coming from the in-phase and the quadrature mixers, inequalities in the amplitudes of these signals will lead to phase errors in the resultant output components. Similarly, deviation in the phase difference from $\pi/4$ between the local oscillator signals injected into the two mixers will cause differing amplitudes of the output components.

The modulator in Fig. 1 can also operate as a QPSK demodulator as shown in Fig. 2. Modulated signals entering the splitter are separated into two equal components and mix with the two subharmonic local oscillator components offset in phase from each other to produce baseband NRZ bit streams. The voltage of the modulated signal entering each mixer may be represented by

$$v_s \cos(2\omega_p t - n\pi/4 - \Phi) \tag{5}$$

where $n = 1$, 3, 5, or 7 for the four phase states and Φ is an arbitrary phase constant. The local oscillator voltage at each mixer is

$$v_p \cos(\omega_p t - m\pi/4 - \theta) \tag{6}$$

where $m = 0$ for the in-phase mixer and $m = 1$ for the quadrature mixer. The phase angle θ is adjusted to give the appropriate baseband bit streams out of the I and Q ports. This implies phase coherence between the local oscillators for both the modulator and demodulator.

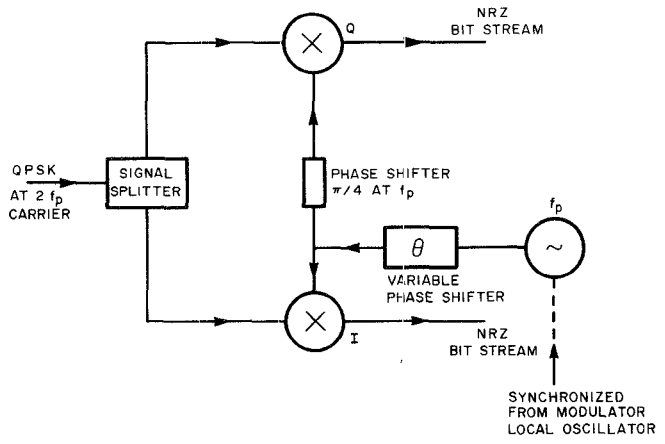


Fig. 2. Schematic view of QPSK demodulator with signal splitter at input, synchronized local oscillator, down-converting mixer circuits, and demodulated NRZ bit streams at the output.

The input voltage at each mixer is then the sum of the modulated signal and local oscillator voltages. After a substitution of the sum of expressions (5) and (6), followed by manipulation with the aid of Bessel function identities [6], the baseband components of the output mixer currents are

$$\begin{aligned} \left.\begin{matrix} i_I \\ i_Q \end{matrix}\right\} = 2i_0 \Bigg[& I_1(kv_s) I_2(kv_p) \\ & \cdot \left\{\begin{matrix} \cos(n\pi/4 + \Phi - 2\theta) \\ \cos(n\pi/4 + \Phi - \pi/2 - 2\theta) \end{matrix}\right\} \\ & + I_3(kv_s) I_6(kv_p) \\ & \cdot \left\{\begin{matrix} \cos 3(n\pi/4 + \Phi - 2\theta) \\ \cos 3(n\pi/4 + \Phi - \pi/2 - 2\theta) \end{matrix}\right\} + \cdots \Bigg] \end{aligned} \tag{7}$$

where $n = 1$, 3, 5, or 7 corresponding to the phase state of the input signal. As in (4) I_1, I_2, I_3, and I_6 are modified Bessel functions which decrease rapidly in relative magnitude with increasing order. Thus only the first term in (7) need be retained, giving

$$\left.\begin{matrix} i_I \\ i_Q \end{matrix}\right\} = 2i_0 I_1(kv_s) I_2(kv_p) \left\{\begin{matrix} \cos(n\pi/4 + \Phi - 2\theta) \\ \cos(n\pi/4 + \Phi - \pi/2 - 2\theta). \end{matrix}\right. \tag{8}$$

For recovery of the original bit streams without crosstalk, $\Phi - 2\theta$ must be zero. If, however, $\Phi - 2\theta$ is a multiple between 1 and 3 of $\pi/2$, the bit streams are separated from each other but emerge from opposite ports or are changed in sign or both.

As in the modulator, nonideal components in the demodulator introduce distortions in the output bit streams. Unequal splitting of the signals at the input of the demodulator or different conversion losses in the two mixers gives unequal amplitudes at the I and Q ports. If the phase

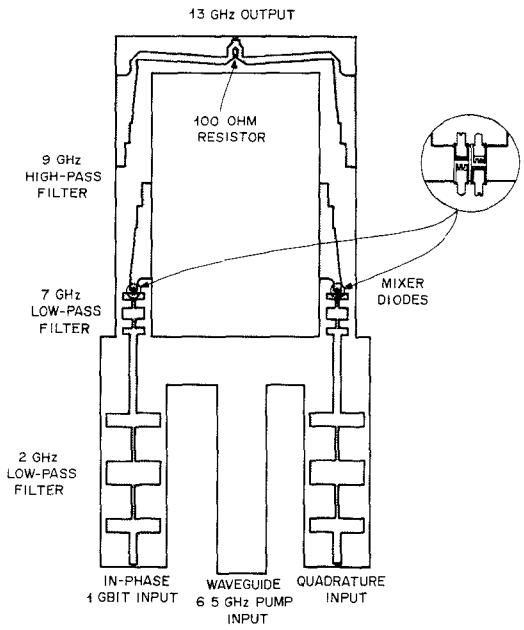


Fig. 3. Top view of dielectric substrate with conductor pattern. The filter structures include 2 GHz and 7 GHz low-pass filters for the incoming bit streams, and a 9 GHz high-pass filter for the up-converted signals. A Wilkinson power adder is used for the summing network at the 13 GHz output.

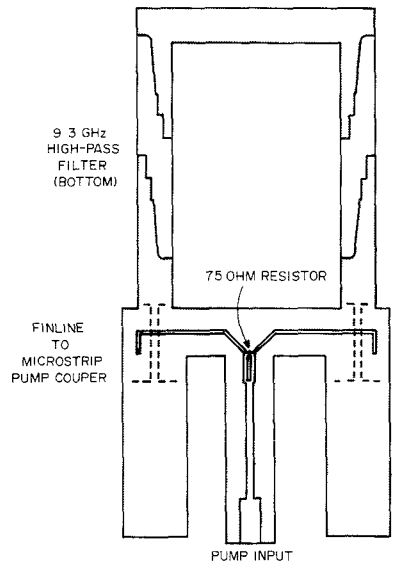


Fig. 4. Conductor pattern on the bottom of the dielectric substrate. The pump power propagates in a finline, splits in a power divider, and is coupled to the microstrip transmission line on the top side through the dielectric substrate.

difference between the local oscillator signals injected into the I and Q mixers is not $\pi/4$, both bit streams cannot be recovered without some crosstalk. It is possible to remove or reduce these distortions by processing the emergent bit streams.

III. Circuit Realization

The QPSK modulator shown schematically in Fig. 2 is built on a dielectric substrate which has etched conductor patterns on both the top and the bottom surface. The substrate, RT/Duroid 5880, has a relative dielectric constant of 2.20, a thickness of 0.031 in, and an electrodeposited copper cladding with a thickness of 0.0012 in (1 oz/ft^2). The substrate is inserted into an aluminum housing which has two coaxial connector inputs for the incoming bit streams, a rectangular waveguide input port for the local oscillator at 6.5 GHz, and a coaxial output for the modulated 13 GHz carrier.

Fig. 3 shows the shape of the dielectric carrier with the top conductor pattern. The conductor pattern on the bottom of the substrate is shown in Fig. 4. The incoming data streams are first transmitted through two low-pass filters with a cutoff frequency of 2 GHz. These five-section $L-C$ microstrip filters are needed to prevent the 6.5 GHz local oscillator power from reaching the input ports of the data streams. The local oscillator input is shown at the bottom of Fig. 4. The waveguide mode at the input is transformed to a finline mode by means of a stepped impedance transformer. A finline power divider is used to transmit half the pump power to each mixer circuit. The finline sections are etched into the ground plane of the Duroid substrate. In order to achieve the required phase shift of $\pi/4$ shown in Fig. 1 in one arm of the pump circuit, it is necessary that the lengths of the finline sections after the power divider be different. The lengths of the horizontal finline sections shown in Fig. 4 differ by $\lambda_P/8$, where λ_P is the wavelength in the finline. The local oscillator power traveling in the horizontal sections of the finlines in Fig. 4 is coupled to the microstrip lines by means of finline-to-microstrip couplers.

Both data streams and the pump power are transmitted through low-pass filters to the mixer diodes for up-conversion to a 13 GHz carrier. The cutoff frequency of each low-pass filter is 6.6 GHz, which permits transmission of the pump but rejects the up-converted and modulated carrier at 13 GHz. The frequency conversion is performed with commercially available beam-leaded Schottky diodes (HP types HSCH-5311 and HSCH-5510) which are connected in antiparallel to achieve the desired hyperbolic sine current-voltage characteristic. A high-pass filter with a cutoff frequency of 9.3 GHz transmits the modulated carrier and provides the dc return for the bit streams. Each filter consists of two antipodal finline transitions from microstrip to waveguide, described by Rubin and Saul [7], arranged back to back. Lower frequencies are rejected by the resulting section of cutoff waveguide. The modulated carriers are subsequently added in a Wilkinson power adder, and the sum appears at the output terminal of Fig. 3.

IV. Performance

Phase and magnitude of the modulator output were measured with dc signals on the I and Q ports to verify operation of the device. The test arrangement in Fig. 5 was used to measure both relative phase and amplitude. A direct measurement of modulator output power with the spectrum analyzer established a power level reference.

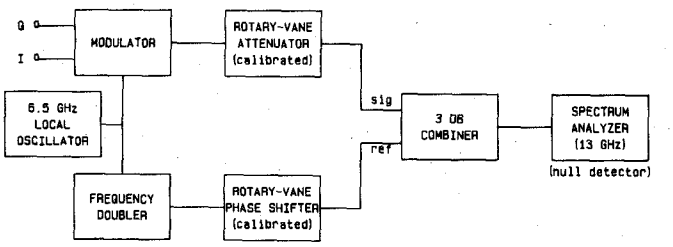


Fig. 5. Schematic diagram of modulator phase and amplitude test set. The dc signals are applied to the input I and Q ports of the modulator. A reference carrier is used as a phase and amplitude reference for measuring phase and amplitude at the output of the modulator.

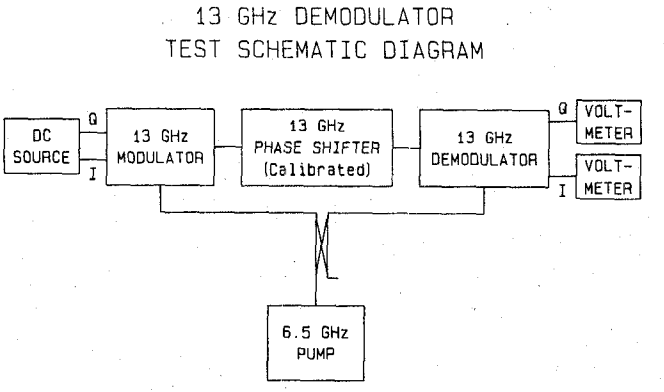


Fig. 6. Phase and amplitude test set for measuring the performance of the demodulator as a function of dc inputs at the I and Q input ports.

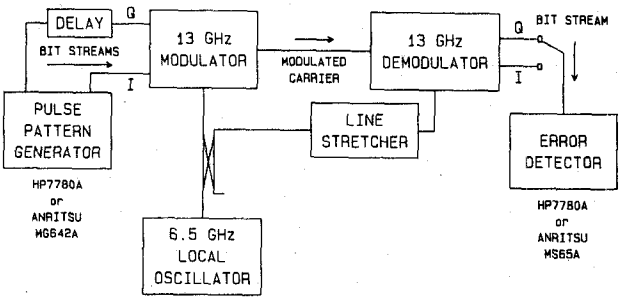
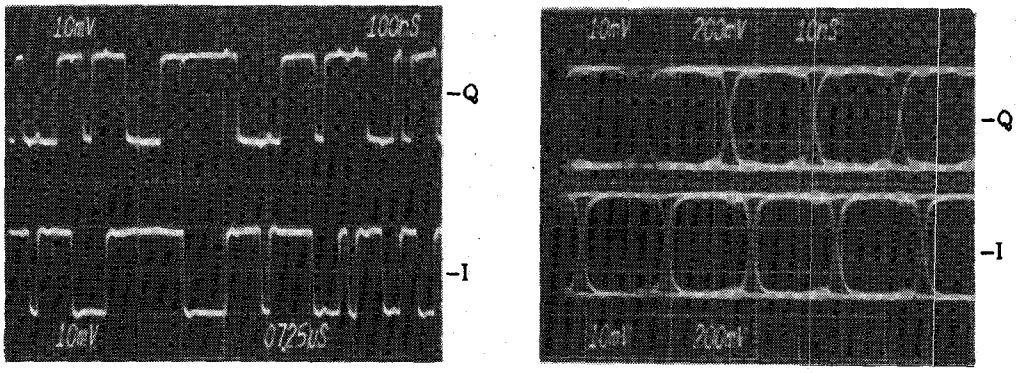
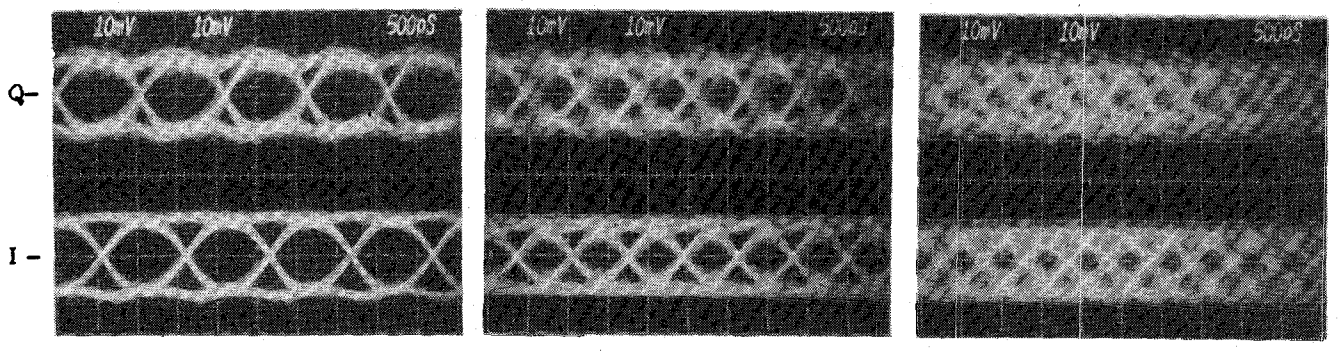


Fig. 7. Schematic diagram of test setup for measuring bit error rates for a 13 GHz modulator and demodulator.



DATA TRAINS EYE DIAGRAMS

Fig. 8. Output pulse trains and eye diagrams measured at I and Q output ports of a modulator–demodulator circuit.



1.0 Gbit/s 1.5 Gbit/s 2.0 Gbit/s

Fig. 9. Output pulse waveforms (eye diagrams) for modulator–demodulator circuits at data rates from 1 to 2 Gbit/s on each rail.

Four similar circuits were measured in two housings, and all showed a typical phase deviation of $\pm 2°$ from quadrature between adjacent phase states. All four circuits showed a consistent conversion of phase modulation to amplitude modulation with an alternation in amplitude between adjacent states, but with different amounts of conversion between units. We attribute this AM to PM conversion to improper phasing of the local oscillator at the two mixers. The AM was reduced to less than 1 dB by increasing the phase length on the longer finline local oscillator feeder with a section of Duroid dielectric placed in contact with the fin.

Modulator circuits were operated as demodulators and were tested for orthogonality of the output at the I and Q ports as shown in Fig. 6. The modulator in Fig. 6 operates as a frequency doubler whose phase is varied with the phase shifter, and the dc output voltage at the I and Q ports recorded as a function of phase shifter angle. The I and Q output voltages are sinusoidal functions of the phase angle. Phase differences of the two sinusoids were adjusted to 90° with the addition of a Duroid strip along the long finline local oscillator feed line, as with the modulator.

Bit error rates were measured for data bit streams as high as 2 Gbit/s passing through a modulator-demodulator pair as shown in Fig. 7. The HP7780A test set was used for data rates up to 50 Mbit/s on each rail, and the Anritsu instruments were used up to 2 Gbit/s. Two bit streams for the I and Q inputs were obtained by splitting the output stream from the generator into two parts, one of which was delayed with respect to the other. The line stretcher adjusted the phase between the modulator and demodulator and was set for minimum cross-coupling between I and Q output signals from the demodulator.

Data trains and eye diagrams of the modulator–demodulator pair outputs are shown in Fig. 8 with 50 Mbit/s pseudorandom input data streams from the HP7780A pulse pattern generator. Some crosstalk is evident by sharp pulses in each data train when the state of the other train changes. Eye diagrams in Fig. 8 are open, and transitions are well defined with bit error rates lower than 10^{-11}. Eye diagrams in Fig. 9 are relatively clean up to 1.5 Gbit/s but are quite diffuse at 2 Gbit/s. Error rates are smaller than 10^{-11} up through 1.5 Gbit/s rising to 5×10^{-3} at 2 Gbit/s. The low-pass filters on the I and Q ports cut off at 1.9 GHz, causing the degradation in performance at 2 Gbit/s.

TABLE I

13 GHz QPSK MODULATOR - DEMODULATOR	
OPERATING CONDITIONS	
Bit Rate/Rail	0 - 2 Gbit/s
Bit Stream Input Levels	± 90 mV
Bit Stream Output Levels	± 11 mV
Carrier Frequency	12.9 GHz
Local Oscillator	
Frequency	6.45 GHz
Power (Modulator)	4 dBm
(Demodulator)	4 dBm
BIT ERROR RATES	
50 - 1500 Mbit/s:	$< 10^{-11}$
2000 Mbit/s:	$\leq 5*10^{-3}$

V. Conclusions

A QPSK modulator operating at a 13 GHz carrier frequency has been built. This modulator can also be operated as a demodulator. Typical operating conditions and bit error rates for the combination are summarized in Table I. The modulator–demodulator pair can transmit at information rates to 1.5 Gbit/s for each rail with low error rates. Both modulator and demodulator are subharmonically pumped with proper phasing of the local oscillators for recovery of each signal without crosstalk.

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